FIG. 1

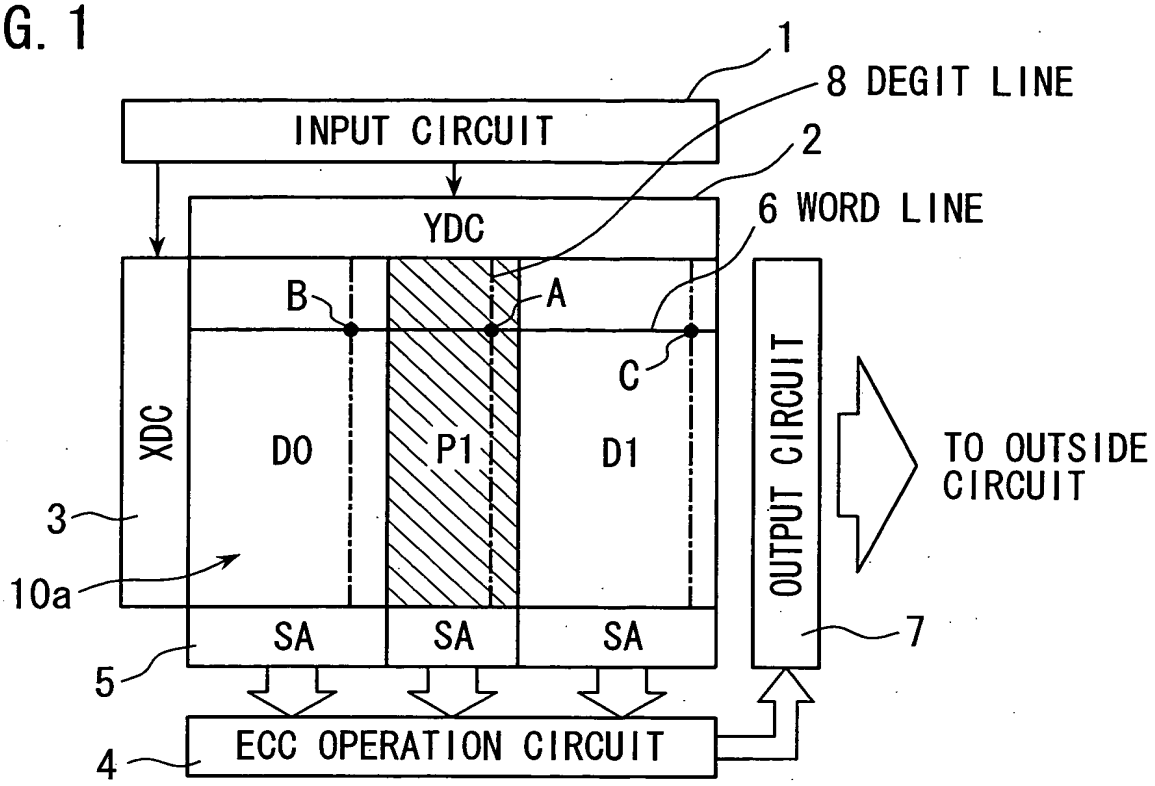


FIG. 2

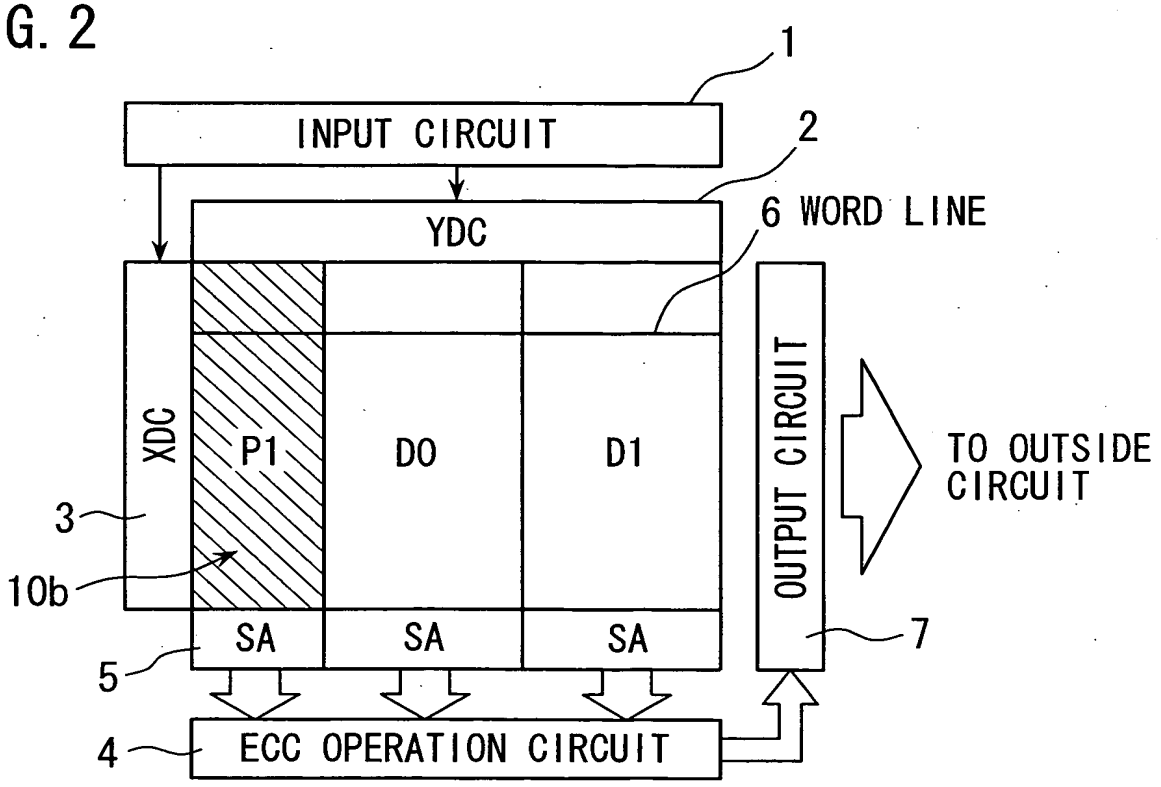
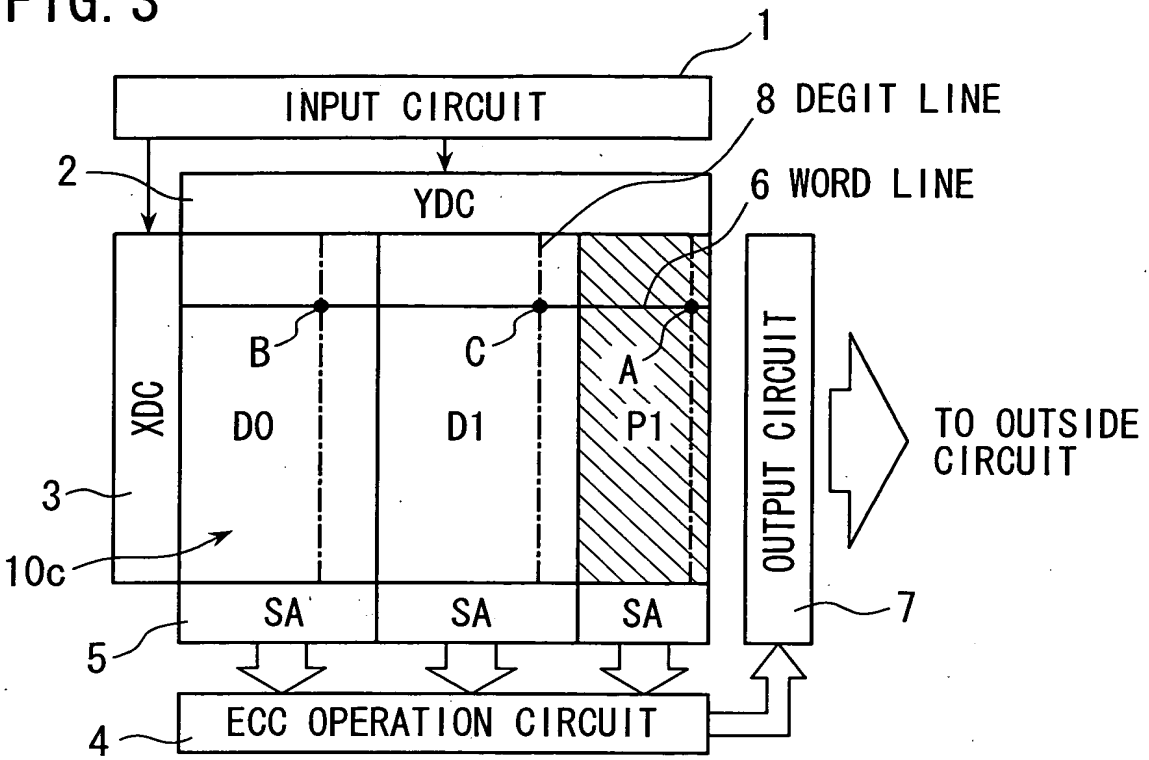
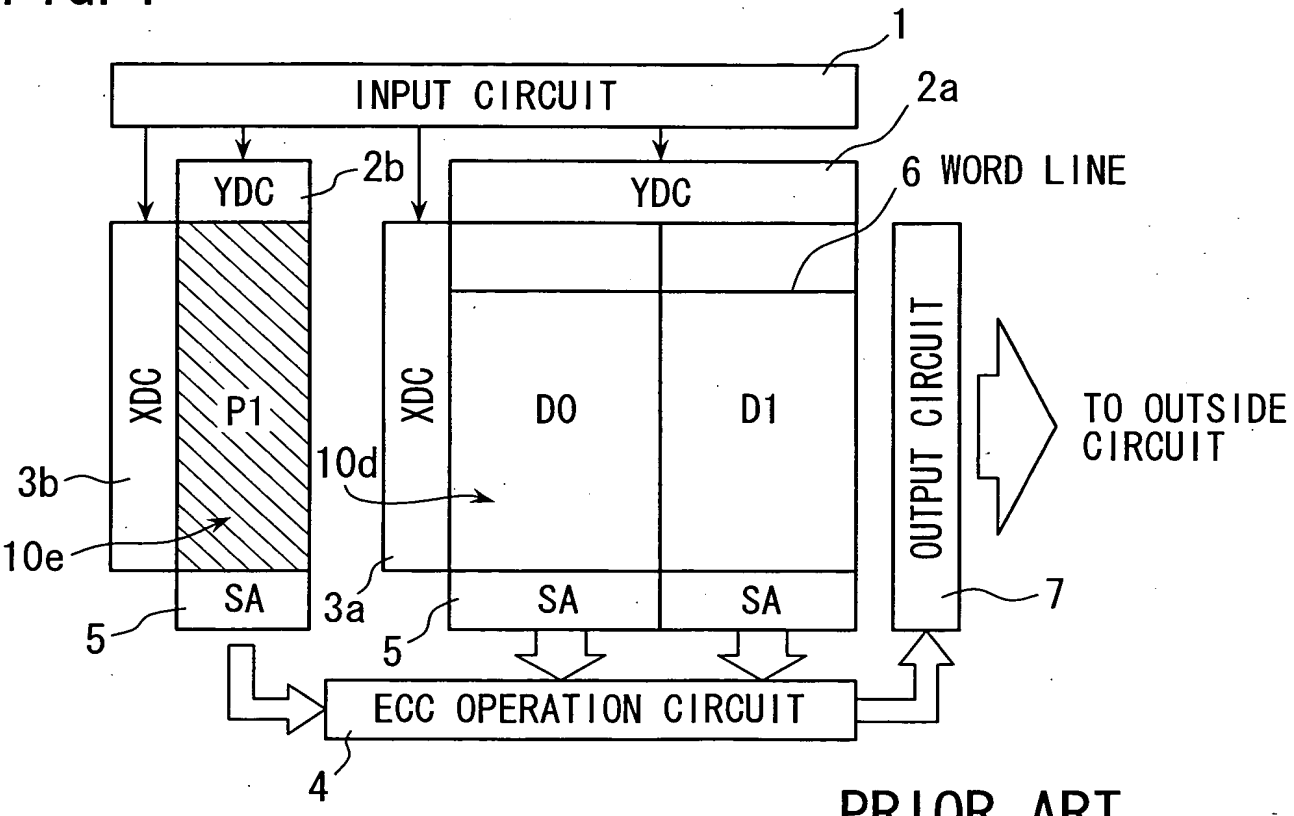


FIG. 3



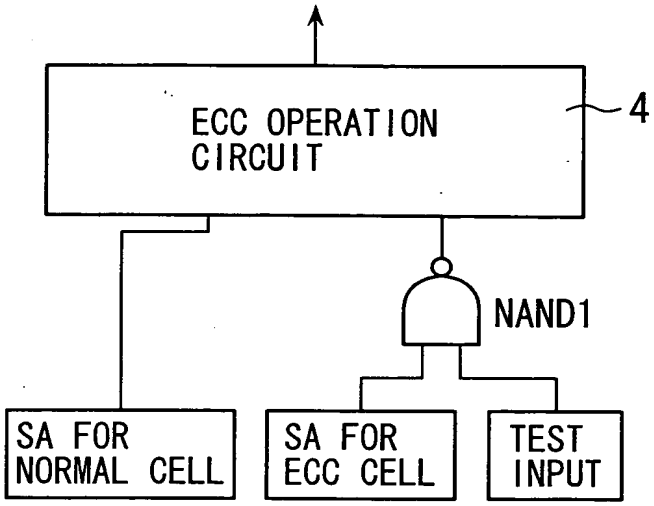
PRIOR ART

FIG. 4



PRIOR ART

FIG. 5



WHEN ECC ENABLED:
TEST INPUT IS VCC → OUTPUT OF NAND1 DEPENDS ON ECC CELL DATA

WHEN ECC DISABLED:
TEST INPUT IS GND → OUTPUT OF NAND1 IS ALWAYS HIGH

PRIOR ART